Refine Search

Your wildcard search against 10000 terms has yielded the results below.
Your result set for the last L# is incomplete.
The probable cause is use of unlimited truncation. Revise your search strategy to use limited truncation.

Search Results -

Terms	Documents
L13 same (map$ or remap$)	4

Database: US Pre-Grant Publication Full-Text Database; US Patents Full-Text Database; US OCR Full-Text Database; EPO Abstracts Database; JPO Abstracts Database; Derwent World Patents Index; IBM Technical Disclosure Bulletins

Search: L14

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Wednesday, January 04, 2006 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L14	L13 same (map$ or remap$)	4	L14
L13	L12 same redundant	82	L13
L12	register adj1 file	10402	L12
L11	L1 same faulty	0	L11
L10	L3 same redundant	0	L10
L9	L1 same redundant	1	L9
L8	L6 same redundant	0	L8
L7	L2 same (map$ or remap$)	15	L7
L6	L1 same map$	46	L6
L5	L3 same map$	0	L5
L4	L3 same logical same physical	0	L4

L3	L2 same register	40	L3
L2	L1 same address$	147	L2
L1	predecod$ adj2 instruction	445	L1

END OF SEARCH HISTORY

L7: Entry 1 of 15 File: USPT Oct 1, 2002

DOCUMENT-IDENTIFIER: US 6460132 B1
TITLE: Massively parallel instruction predecoding

Detailed Description Text (26):
Turning now to FIG. 4, details of one embodiment of prefetch/predecode unit 12 are shown. As the figure illustrates, prefetch/predecode unit 12 may include a prefetch unit 60, a plurality of predecode units 62A-D, and a start/end fixer/sorter unit 64 (also referred to herein as a prefix bit correction unit or simply as a correction unit). Prefetch unit 60 is configured to output a prefetch address (e.g., from branch prediction unit 14) to the computer system's main memory subsystem. Several clock cycles later, the corresponding instruction bytes become available on bus 66. Bus 66 may be configured to route a first subset of the instruction bytes to predecode unit 62A, a second subset of the instruction bytes to predecode unit 62B, a third subset of the instruction bytes to predecode unit 62C, and a fourth subset of instruction bytes to predecode unit 64D. In some embodiments, this may be accomplished through the use of buffers (e.g., FIFOs) and routing logic (not shown). Prefetch unit 60 may also be configured to route the prefetch address information to one or more of the predecode units 62A-D or routing logic on bus 66. To simplify the necessary hardware, many x86 microprocessors fill entire lines in the instruction cache at once, with the restriction that each cache line can only be mapped to aligned blocks of main memory (e.g., 128-bit blocks). Aligned 128-bit blocks begin at addresses that have the lower four bits clear. Thus, by also routing the prefetch address to the predecoders, the predecoders may use the offset portion of the address to predecode the instruction bytes regardless of whether the first complete instruction begins at the start of the aligned block or in the middle of the aligned block.

L14: Entry 3 of 4 File: JPAB Jun 18, 1993

DOCUMENT-IDENTIFIER: JP 05150981 A
TITLE: DATA PROCESSOR

Abstract Text (2):
CONSTITUTION: This device is provided with a visible register map for connecting a physical register with a logical register, and this is constituted of a processing unit 10, memory 12, and register file RF 14 equipped with one set of physical hardware registers. The memory 12 is constituted as the combination of a main memory 15 and a cache memory 16. In this case, an instruction including the transfer of data between the registers evades a logically redundant arithmetic operation, and those instructions are removed from the longest execution path. That is, a data processing is executed by changing a connection relation between the physical register and the logical register without actually transferring the data between the registers.